a plurality of dynamic memory cells, each of which is coupled to one of said word lines and to one of said data lines;

an amplifier, coupled to said pair of data lines, adapted to amplify a potential difference between said data lines so as to provide said data lines with a high-level potential and a low-level potential, respectively, wherein said amplifier includes a pair of N-channel MOS transistors and a pair of P-channel MOS transistors, wherein each transistor of said pair of N-channel MOS transistors has a gate cross-coupled to a drain of the other transistor of said pair of N-channel MOS transistors, wherein a drain of one of said pair of N-channel MOS transistors is coupled to one of said pair of data lines and the drain of the other of said pair of N-channel MOS transistors is coupled to the other of said pair of data lines, wherein each transistor of said pair of P-channel MOS transistors has a gate cross-coupled to a drain of the other transistor of said pair of P-channel MOS transistors, and wherein a drain of one of said pair of P-channel MOS transistors is coupled to one of said pair of data lines and the drain of the other of said pair of P-channel MOS transistors is coupled to the other of said pair of data lines; and

a precharging circuit adapted to set said data lines at a predetermined level when said plurality of dynamic memory cells are in a non-selected state, wherein said predetermined level is an intermediate level between said high-level potential and said low-level potential.

A2 Contd

21. 2 A semiconductor memory according to claim 20, 1 further comprising:

a first switching MOS transistor of N-channel type having a drain coupled to a source of each of said pair of N-channel MOS transistors and a source coupled to a first potential terminal; and

Q2 Contd a second switching MOS transistor of P-channel type having a drain coupled to a source of each of said pair of P-channel MOS transistors and a source coupled to a second potential terminal.

3 2
22. A semiconductor memory according to claim 21,

wherein said precharging circuit includes a third switching MOS transistor having a source-drain path provided between said pair of data lines, and

wherein said third switching MOS transistor is controlled so that said pair of data lines are electrically coupled to each other when said plurality of dynamic memory cells are in said non-selected state.

4 3
23. A semiconductor memory according to claim 22,

wherein said first potential terminal has a potential level corresponding to said low-level potential, and

wherein said second potential terminal has a potential level corresponding to said high-level potential.

5 4
24. A semiconductor memory according to claim 23, further comprising a control circuit adapted to supply control